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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/353,120	07/14/1999	LOUIS F. VILLAROSA JR.	061607-1100	3012

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EXAMINER

KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
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2631

DATE MAILED: 07/09/2004

21

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/353,120

Applicant(s)

VILLAROSA ET AL.

Examiner

Pankaj Kumar

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7, 10-16, 19-22, 25 and 27-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-7, 10, 16, 19-20, 27 and 28 is/are allowed.
- 6) ☒ Claim(s) 11-15, 25 and 29 is/are rejected.
- 7) ☒ Claim(s) 21 and 22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 11-15, 25 and 29 have been considered but are moot in view of the new ground(s) of rejection.
2. The amendments to claims previously cited to be allowable do not affect their status except an objection to the numbering of claims 21 and 22.

Response to Amendment

Claim Objections

3. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Accordingly, claims 21 and 22 are objected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, 12, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hedberg USPN 5,526,361.

5. As per claim 11, Hedberg shows a method for detecting errors in the synchronization of a DTE data signal (Hedberg fig. 3: Din) with a DCE clocking signal (Hedberg fig. 3: CKout) in a communication environment wherein the DCE (Hedberg element where CKout is going from fig. 3) interfaces the DTE (Hedberg element outputting Din which is input into fig. 3) to a communication channel, the method comprising the steps of:

- a. providing a master clock signal (Hedberg fig. 3: CKin);
- b. deriving a DCE clocking signal (Hedberg fig. 3: CKout) and an internal clocking signal (Hedberg fig. 3: output of delta Ts) from said master clocking signal (Hedberg fig. 3: CKin), said internal clocking signal ~~having the same frequency as the~~ and said DCE clocking signal (Hedberg: Summary section including "... first combining means for combining the phase shifted signals in groups for obtaining a number of pulses with a length corresponding to the phase shift between the outputs of the corresponding group and the same frequency as that of the reference signal ... ") having a first frequency that is a fraction of the frequency of the master clock signal (Hedberg: fig. 20 shows X is CK out. Fig. 21 shows X has a frequency which is a 2/1 fraction of CKin. Figs. 15 and 16 show output of delta Ts have a frequency which is a 1/1 fraction of the CK in signal. Figures 15 and 16 also show X has a frequency which is a 2/1 fraction of CKin and X from fig. 21 is CKout.);
- c. obtaining a first sample of said DTE data signal at a first time a second sample of said DTE data signal at a second time, said second time being subsequent to said first

time, the time interval between said first time and said second time being less than the period of the DCE clocking signal (Hedberg fig 3: 55 just rotates clock between 0 and 360 degrees. Suppose it rotates it 90 degrees, that means the clock will be shifted a little but the shift will be less than 1 period length.)

d. comparing said first sample to said second sample and determining whether the DTE data signal has undergone a transition during the time interval between the first time and the second time. (Hedberg: for the remaining portions of the claim, see figs. 3, 3a, paragraph 20: "The output signals of D-flip-flops 70 and 72 are associated with A and C, respectively in FIG. 3a, whereas the output signal from the flip-flop 92 is associated with B. By carrying through these three readings and comparing them it is possible to see how the reading points are located in the "data eye". If the reading occurs too early, A will deviate from B, which results in the gate 74 emitting a signal implying that the clock phase should be increased. Correspondingly C will deviate at late reading resulting in the gate 76 emitting a signal implying that the clock phase should be decreased. ")

6. As per claim 12, the method of claim 11 wherein the interval between said first time and said second time is approximately $1/8$ of the period of the DCE clocking signal (Hedberg fig. 3: when element 55 rotates the clock by 90 degrees, the interval between the first time and second time will be $1/4$ of the period of the DCE clocking signal and $1/4$ is approximately $1/8$).

7. As per claim 13, the method of claim 11, further comprising the step of generating a selector control signal if said first sample is different from said second sample (Hedberg: figs. 3,

3a, paragraph 20: "The output signals of D-flip-flops 70 and 72 are associated with A and C, respectively in FIG. 3a, whereas the output signal from the flip-flop 92 is associated with B. By carrying through these three readings and comparing them it is possible to see how the reading points are located in the "data eye". If the reading occurs too early, A will deviate from B, which results in the gate 74 emitting a signal implying that the clock phase should be increased. Correspondingly C will deviate at late reading resulting in the gate 76 emitting a signal implying that the clock phase should be decreased. ").

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 14, 15, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hedberg.

10. As per claim 14, the method of claim 13, further comprising the steps of: inverting said circuit clocking signal to produce an inverted circuit clocking signal (Hedberg fig. 12: CK90 is an inversion of CK0 shifted by 90 degrees. If another shift of 90 degrees is made then this will be an inversion); and producing said internal clocking signal that is selected in response to said selector control signal, from the group consisting of said DCE clocking signal and said inverted clocking signal (not in Hedberg since Hedberg can choose DCE clocking signal, inverted clocking signal (i.e. shift of 180 degrees) or shift of 90 degrees; however, it would have been

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obvious to one skilled in the art at the time of the invention to modify Hedberg to only teach DCE clocking signal or inverted clocking signal since lacking any criticality, to eliminate prior art parts (i.e. only keeping the 0 degree and 180 degree choice and removing the 90 degree choice) and its function does not make the claimed invention patentable over that prior art (In re Karlson, 153 USPQ 184). Also, lacking any criticality, changing the proportion of prior art parts (i.e. only have a 0 degree choice or a 180 degree choice and not a 90 degree choice) does not make the claimed invention patentable over that prior art (In re Reese, 129 USPQ 402). Also, lacking any criticality, changing the size or range (i.e. only have a 0 degree choice or a 180 degree choice and not a 90 degree choice) of the prior art parts does not make the claimed invention patentable over that prior art (In re Rose, 105 USPQ 237).)

11. As per claim 15, the method of claim 14 further comprising the step of latching said DTE data signal (Hedberg: inherent for the data to be latched in the flip flops)

12. As per claim 25, the method of claim 15 further comprising the step of performing said obtaining step and said latching step according to a time sequence referenced to said internal clocking signal (Hedberg fig. 3: flip flops obtain and latch the data according to internal clocks which are delayed).

13. As per claim 29, the method of claim 13, further comprising the steps of: inverting said internal clocking signal to produce an inverted circuit clocking signal; and producing said DCE

clocking signal that is selected in response to said selector control signal, from the group consisting of said internal clocking signal and said inverted clocking signal. (discussed above)

14. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gutttag 6,232,955

15. As per claim 11, Gutttag teaches a method for detecting errors in the synchronization of a DTE data signal with a DCE clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of (preamble is not afforded patentable weight):

- e. providing a master clock signal (Gutttag fig. 33: DOTCLK);
- f. deriving a DCE clocking signal (Gutttag fig. 33: VCLK) and an internal clocking signal (Gutttag fig. 34: SCLK) from said master clocking signal, said internal clocking signal ~~having the same frequency as the~~ and said DCE clocking signal having a first frequency that is a fraction of the frequency of the master clock signal (Gutttag fig. 33: VCLK and SCLK have frequencies which are a fraction of the DOTCLK frequency);
- g. obtaining a first sample of said DTE data signal at a first time (Gutttag fig. 47: 20) a second sample of said DTE data signal at a second time (Gutttag fig. 47: 21) (portion for this not in Gutttag but it would be obvious as explained below), said second time being subsequent to said first time (Gutttag fig. 47: 21 is after 20), the time interval between said first time and said second time being less than the period of the DCE clocking signal (Gutttag fig. 47: 20 and 21 occur within one DOTCLK period)
- h. comparing said first sample to said second sample and determining whether the DTE data signal has undergone a transition during the time interval between the first time

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and the second time (Guttag teaches pixel bits p0 to p31 and as these pixel bits are used for display purposes, a person would be able to visually see the transition of the image between two times).

16. Although Guttag teaches data over a time period under the DOTCLK, Guttag does not teach obtaining a first sample of said DTE data signal at a first time a second sample of said DTE data signal at a second time. It is common knowledge that since data exists, data will be obtained. It would have been obvious to one skilled in the art at the time of the invention to modify Guttag to teach that the data will be obtained. One would have been motivated to do so in order for Guttag to be efficient - since it is working with data, if it does not obtain the data, the data is wasted.

Allowable Subject Matter

- 17. Claims 1-7, 10, 16, 19-20, 27-28 are allowed.
- 18. See an earlier action for details.
- 19. Claims 21 and 22 are objected.

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER

3/1/04

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Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Mon, Tues, Wed and Thurs after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (703) 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PK